WHAT IS CLAIMED IS:

1. A packet switch formed by connecting unit switches in multi-stages, wherein

a unit switch at the first stage assigns a sequence number to an input packet according to a destination of the packet and distributes and sends out the packet to a unit switch at a succeeding stage, and

a unit switch at the final stage sequences and outputs a packet received from a unit switch at a preceding stage according to a sequence number assigned to the packet.

2. The packet switch as set forth in claim 1, wherein

said unit switch at the first stage assigns, to an input packet, a sequence number set for each combination of a unit switch which has received input of the packet and a unit switch which finally outputs the packet, as well as assigning identification information about its own switch which is a unit switch having received input of said packet.

3. The packet switch as set forth in claim 1, wherein

the total number of sequence numbers to be assigned by said unit switch at the first stage to an

input packet is set based on a maximum value of a queuing delay at a unit switch at the succeeding stage and the number of input and output ports of the unit switch in question at the succeeding stage.

4. The packet switch as set forth in claim 1, wherein

said unit switch at the first stage assigns, to an input packet, a sequence number set for each combination of a unit switch which has received input of the packet and a unit switch which finally outputs the packet, as well as assigning identification information about its own switch which is a unit switch having received input of said packet, and

said unit switch at the final stage

includes queues provided for the respective unit switches at the first stage which receive input of packets and slotted on a packet basis,

based on said identification information and said sequence number assigned to a packet arriving from a unit switch at the preceding stage, writes the packet in question into a corresponding slot of corresponding one of said queues, and

sequentially reads and outputs said packets written in said queues according to the order of said sequence numbers.

5. The packet switch as set forth in claim 4, wherein

said unit switch at the final stage determines an initial value of a read pointer for said queue based on a sequence number of a packet received first.

6. The packet switch as set forth in claim 4, wherein

when a packet is read from a slot indicated by a read pointer in said queue or when no packet arrives at the slot indicated by the read pointer in said queue for a predetermined time period, said unit switch at the final stage updates the read pointer in question.

7. The packet switch as set forth in claim 4, wherein

said unit switch at the final stage

determines an initial value of a read pointer for said queue based on a sequence number of a packet received first, and

when a packet is read from a slot indicated by a read pointer in said queue or when no packet arrives at the slot indicated by the read pointer in said queue for a predetermined time period, updates the read pointer in question.

8. The packet switch as set forth in claim 1,

wherein

said unit switch comprises:

a 2Nx2 switch unit having a number 2N of input ports and a number N of output ports,

a packet distribution unit for assigning, to an input packet, a sequence number according to a destination of the packet and distributing and sending out the packet to a unit switch at a succeeding stage,

a packet alignment unit for sequencing, according to a sequence number assigned to a packet received from a unit switch at a preceding stage, a packet and transferring the sequenced packets to said 2NxN switch unit, and

a filter for distributing input packets into packets to be returned within its own switch and packets to be sent out to a unit switch at a succeeding stage and transferring said packets to be returned to said 2NxN switch unit and transferring said packets to be sent to a switch at a succeeding stage to said packet distribution unit.

9. The packet switch as set forth in claim 8, wherein

said packet distribution unit at said unit switch at the first stage assigns, to an input packet, a sequence number set for each combination of a unit switch which has received input of the packet and a unit

switch which finally outputs the packet, as well as assigning identification information about its own switch which is a unit switch having received input of said packet.

10. The packet switch as set forth in claim 8, wherein

the total number of sequence numbers to be assigned by said packet distribution unit in said unit switch at the first stage to an input packet is set based on a maximum value of a queuing delay at a unit switch at the succeeding stage and the number of input and output ports of the unit switch in question at the succeeding stage.

11. The packet switch as set forth in claim 9, wherein

said unit switch at the final stage includes queues provided for the respective unit switches at the first stage which receive input of packets and slotted on a packet basis,

based on said identification information and said sequence number assigned to a packet arriving from a unit switch at a preceding stage, said packet alignment unit writes the packet in question into a corresponding slot of corresponding one of said queues, and

said 2NxN switch unit sequentially reads and

outputs said packets written in said queues according to the order of said sequence numbers.

12. The packet switch as set forth in claim 11, wherein

said unit switch at the final stage determines an initial value of a read pointer for said queue based on a sequence number of a packet received first.

13. The packet switch as set forth in claim 11, wherein

when a packet is read from a slot indicated by a read pointer in said queue or when no packet arrives at the slot indicated by the read pointer in said queue for a predetermined time period, said unit switch at the final stage updates the read pointer in question.

14. The packet switch as set forth in claim 11, wherein

said unit switch at the final stage

determines an initial value of a read pointer for said queue based on a sequence number of a packet received first, and

when a packet is read from a slot indicated by a read pointer in said queue or when no packet arrives at the slot indicated by the read pointer in said queue for a predetermined time period, updates the read pointer in

question.